SYSTEM

User Guide

CD1-OPERA • *CompactPCI®* 6U P4-M CPU

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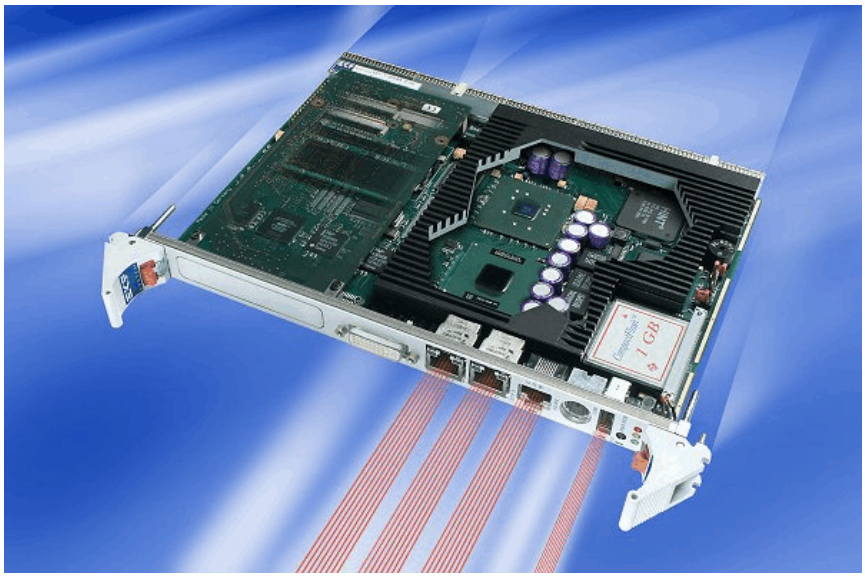

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About this Manual

This manual describes the technical aspects of the CD1-OPERA, required for installation and system integration. It is intended for the experienced user only.

Edition History

Ed.	Contents/*Changes*	Author	Date
1	User Manual CD1-OPERA English (text #2751, file: cd1_uge.wpd) Initial edition, to be completed later on.	gn	2002-10-24
2	Changed IDs of local PCI devices according to rev. 1 of the board.	gn	2003-06-10
3	Changes to table "Feature Summary" (Typical Power Consumption, BIOS).	jj	15 August 2003
4	Changed table "Feature Summary". Removed table "Ordering Information". Changed Block Diagram and Top View. Changed table "Strapping Headers". Changed table "Connectors and Sockets". Changed tables in sections "Microprocessor" and "Thermal Considerations". Changed section "Enhanced IDE Interface". Changed section "Universal Serial Bus (USB)". Changes since programable LED moved from IDE-LED to PWR-LED. Changed factory default of JFWH. Added section "Reset Jumper CMOS Values (JRTC)". Added IDE to MDJ4 mapping table to section "PMC Slot MDJ4". Filled table in section "Power Supply Require-ments". Changed table in section "CompactPCI J4", added footer to table.	gn	2003-09-15
5	Added reference to CDX-RIO in section "Related Documents"	gn	2003-09-29
6	Corrected DRVEN0# to DRVDEN0# in Compact PCI J4 connector table.	gn	2003-09-30
7	Table 'Feature Summary', added rows (environment specs) Table 'Feature Summary', mixing up in row 'IDE/ATA' eliminated	jj	16 October 2003
8	Table 'Feature Summary', added rows (typical calculating performance)	jj	11 February 2004
9	Added image CD1-OPERA & CDX-RIO	jj	14 June 2004
10	Changed table MDJ2 PMC mezzanine connector (BUSMODE[4:2] signals)	jj	17 June 2004
11	Added images on-board hard disk module	jj	23 August 2004

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Related Documents

Features of the Rear-I/O expansion board CDX-RIO are described in the Technical Information 'CDX-RIO • Rear I/O Transition Module' available via the link location

http://www.ekf.de/c/ccpu/cd1/cdx_tie.pdf.

For a description of the CD1-OPERA BIOS see document 'CD1-OPERA PhoenixBIOS User's Manual', available by download at

http://www.ekf.de/c/ccpu/cd1/cd1.html.

Nomenclature

Signal names used herein with an attached '#' designate active low lines.

Trade Marks

Some terms used herein are property of their respective owners, e.g.

Intel, Pentium, Northwood, Brookdale: ® Intel
CompactPCI : ® PICMG
Windows 98, Windows NT, Windows 2000, Windows XP: ® Microsoft

EKF does not claim this list to be complete.

Legal Disclaimer - Liability Exclusion

This manual has been edited as carefully as possible. We apologize for any potential mistake. Information provided herein is designated exclusively to the proficient user (system integrator, engineer). EKF can accept no responsibility for any damage caused by the use of this manual.

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CD1-OPERA Features

Feature Summary

Feature Summary CD1-OPERA	
Form Factor	Double size *CompactPCI* style Eurocard (160x233mm^2), front panel width 4HP (20.3mm)
Processor	Intel® Mobile Pentium® 4 Processor - M (Northwood® 0.13µ generation), clock rate 1.7GHz, 2.2GHz
Chipset	i845G (Brookdale®) chipset consisting of: • 82845G Graphics/Memory Controller Hub (GMCH) • 82801D I/O Controller Hub (ICH4) • 2 x Firmware Hub (FWH) 82802 compatible
Memory	200-pin SO-DIMM socket (notebook style module), PC2100 DDR266-SDRAM, 1GB maximum
Video I/O	Analog monitor and digital flat-panel display support by DVI-I connector (front panel), up to 2048 x 1536 pixel 16M colours 85Hz refresh rate, incorporates PanelLink Digital technology (Silicon Image)
USB I/O	Type A connector (front panel) USB 2.0, another two USB ports across rear I/O (J4)
Ethernet I/O	3 independent 10/100/1000Mbps Gigabit Ethernet controllers, 82540 chip, 2 x RJ-45 connectors available from the front panel, 1 x rear I/O according to PICMG® 2.16 across J3
Legacy I/O	LPC Super-I/O controller on-board, COM1 (front panel), combined PS/2 keyboard and mouse port (front panel), COM2, parallel port, floppy disk interface (rear I/O across J4)
IDE/ATA	• Ultra ATA/100 44-pin connector (secondary IDE, master/slave) • CompactFlash socket for CFA ATA cards (secondary IDE, master) • Primary IDE port available across rear I/O (J4)
PXI Interface	PCI eXtensions for Instrumentation Standard, Rev. 2.0 (rear I/O across J2)
Mezzanine I/O	Stuffed alternatively (ordering options): • 1 slot for a PMC module, I/O from the front panel and across J5 (e.g. CD1-1-OPERA) • 2 slots for PC•MIP modules, I/O from front panel and across J5 (e.g. CD1-2-OPERA) • on-board 2.5" hard disk module, primary IDE (e.g. CD1-4-OPERA)
Rear I/O	• IDE, Floppy, USB2, USB3, LPT, COM2, GPIO (J4) • Gigabit Ethernet (J3) • Mezzanine Rear I/O (J5) • Rear I/O transition module available (CDX-RIO)

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Feature Summary CD1-OPERA			
CompactPCI® Bus	64-bit, 33/66MHz, PCI bridge HINT HB6 (PLX), configurable as CompactPCI system slot controller (e.g. CD1-1-OPERA), or peripheral slot board (e.g. CD1-A-OPERA)		
Hot Swap Function	Board installing and removing without adversely effecting a running system, 'Full Hot Swap' implementation according to CompactPCI Hot Swap Specification PICMG® 2.1 (for peripheral slot boards only, e.g. CD1-A-OPERA)		
Typical Power Consumption	1.7GHz modest load (WinXP) full load (MaxPow80) full load (PCMark2002)	3.3V 2.2A 2.2A 2.9A	5V 0.9A 5.4A 5.4A
	2.2GHz modest load (WinXP) full load (MaxPow80) full load (PCMark2002)	3.3V 2.2A 2.2A 2.9A	5V 1.1A 7.2A 7.2A
	1.2GHz Battery Optimized Mode modest load (WinXP) full load (MaxPow80) full load (PCMark2002)	3.3V 2.2A 2.2A 2.9A	5V 0.7A 3.2A 3.2A
BIOS	Phoenix BIOS 4.0 Rel.6.0, 8/16Mbit Flash (Dual Firmware Hub)		
MTBF	88,000h		
Ambient Temperature	• 0˚C to +60˚C (operating) • -40˚C to +85˚C (storage)		
Relative Humidity	5% to 95% (non condensing)		
Altitude	-300m to +3000m		
Shock	15g 0.33ms, 6g 6ms		
Vibration	1g 5-2000Hz		
Typical Calculating Performance	PCMark2002 under Windows 2000, CPU/MEM Score		
	4132/3931 @1.7GHz	5236/4152 @2.2GHz	

Ordering Information

The CD1-OPERA is available in many different configurations. To get an overview take a look at the price list on EKFs website http://www.ekf.de/liste/liste_20.html, or download the document http://www.ekf.de/c/ccpu/cd1/cd1_pie.pdf.

Short Description CD1-OPERA

Equipped with the Intel® Mobile Pentium® 4 Processor up to 2.2GHz, the CD1-OPERA is a powerful 6U (double size Eurocard) CompactPCI® CPU board.

The board is provided with the chipset 845G (Brookdale®), which contains an embedded graphics controller. The DVI-I interface allows for attachment of both, advanced (digital) and legacy (analog) flat panel displays and CRT monitors. The mobile 0.13µ processor (Northwood®) reduces the power consumption considerably, thus enabling a reliable passive heatsink solution for thermal discharge.

Three USB 2.0 ports allow for plug & play attachment of a variety of peripheral devices. For high speed networking up to 1000Mbps, the CD1-OPERA is equipped with three independent Gigabit Ethernet controllers. The PICMG® 2.16 standard (Ethernet over CPCI backplane) is also supported.

As mass storage interface, the CD1-OPERA provides an Ultra ATA/100 connector. In addition, a receptacle for ATA CompactFlash cards allows utilization of a silicon disk. The main memory is a SO-DIMM 200 form factor DDR-SDRAM module up to 1GB capacity.

The PCI bridge allows for configuring of the CD1-OPERA as a CompactPCI system slot controller, or peripheral slot board in multi-processor applications. Alternatively, either one PMC card socket, or two PC•MIP mezzanine module slots, or a 2.5-inch hard disk module enable on-board expansion of the CD1-OPERA. A local PXI controller is provided for measuring and testing applications. The *Phoenix BIOS* is maintained by EKF. So custom specific enhancements can be realized.

The CD1-OPERA is a high performance industrial CPU, suitable for stand-alone applications as well as large CPCI systems.

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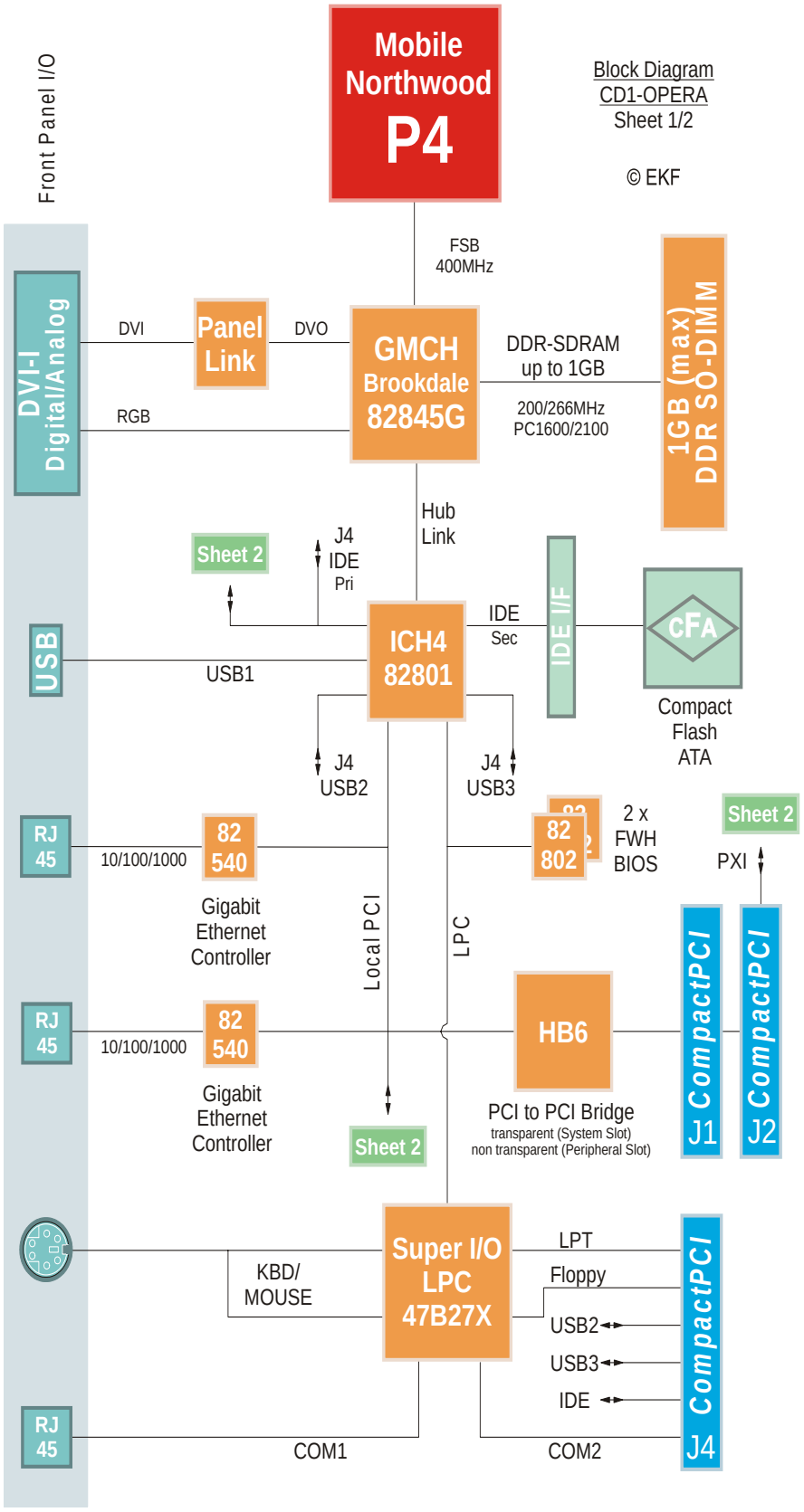
Block Diagram CD1-OPERA



CD1-OPERA Block Diagram (1 of 2)

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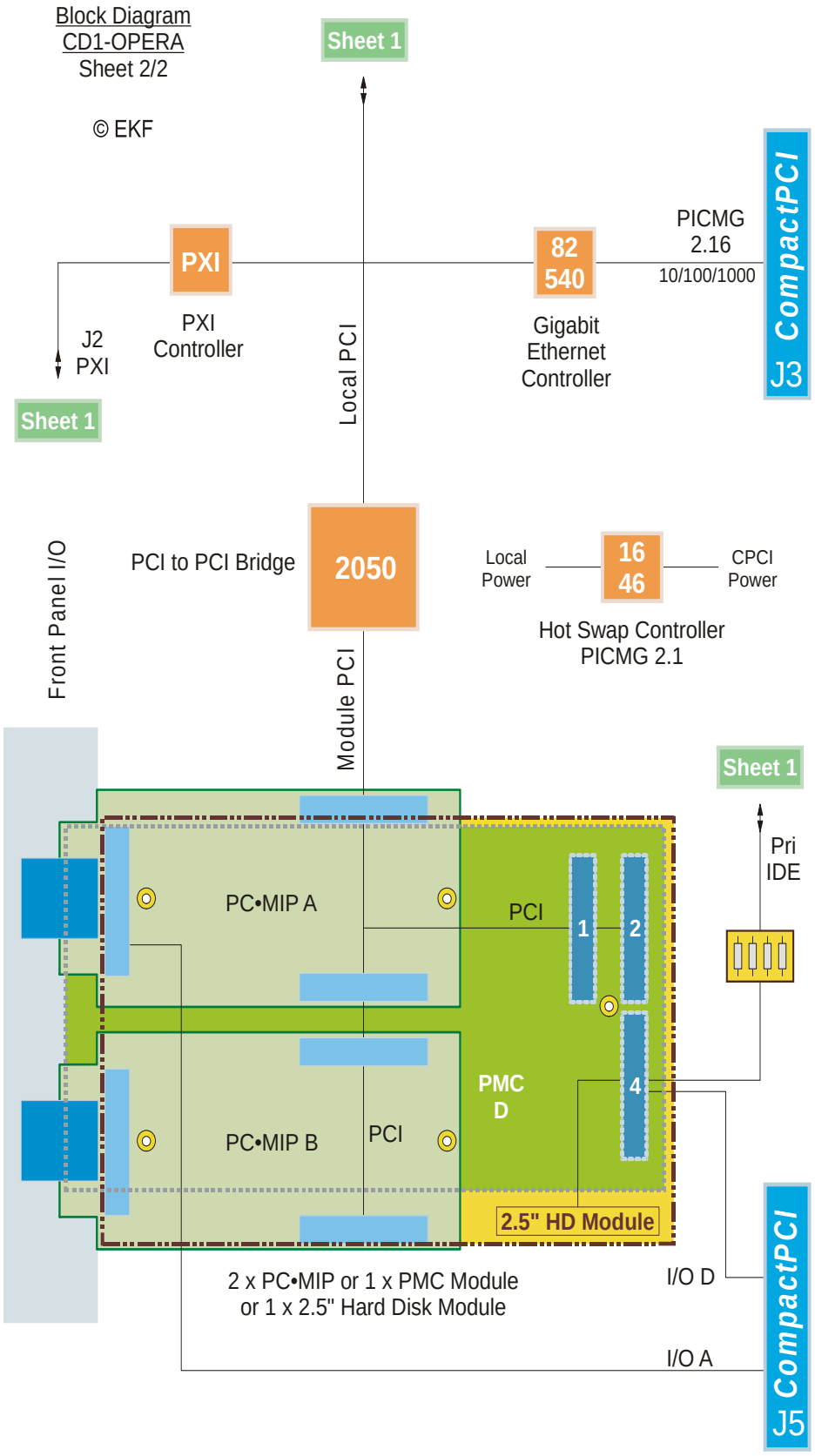

CD1-OPERA Block Diagram (2 of 2)

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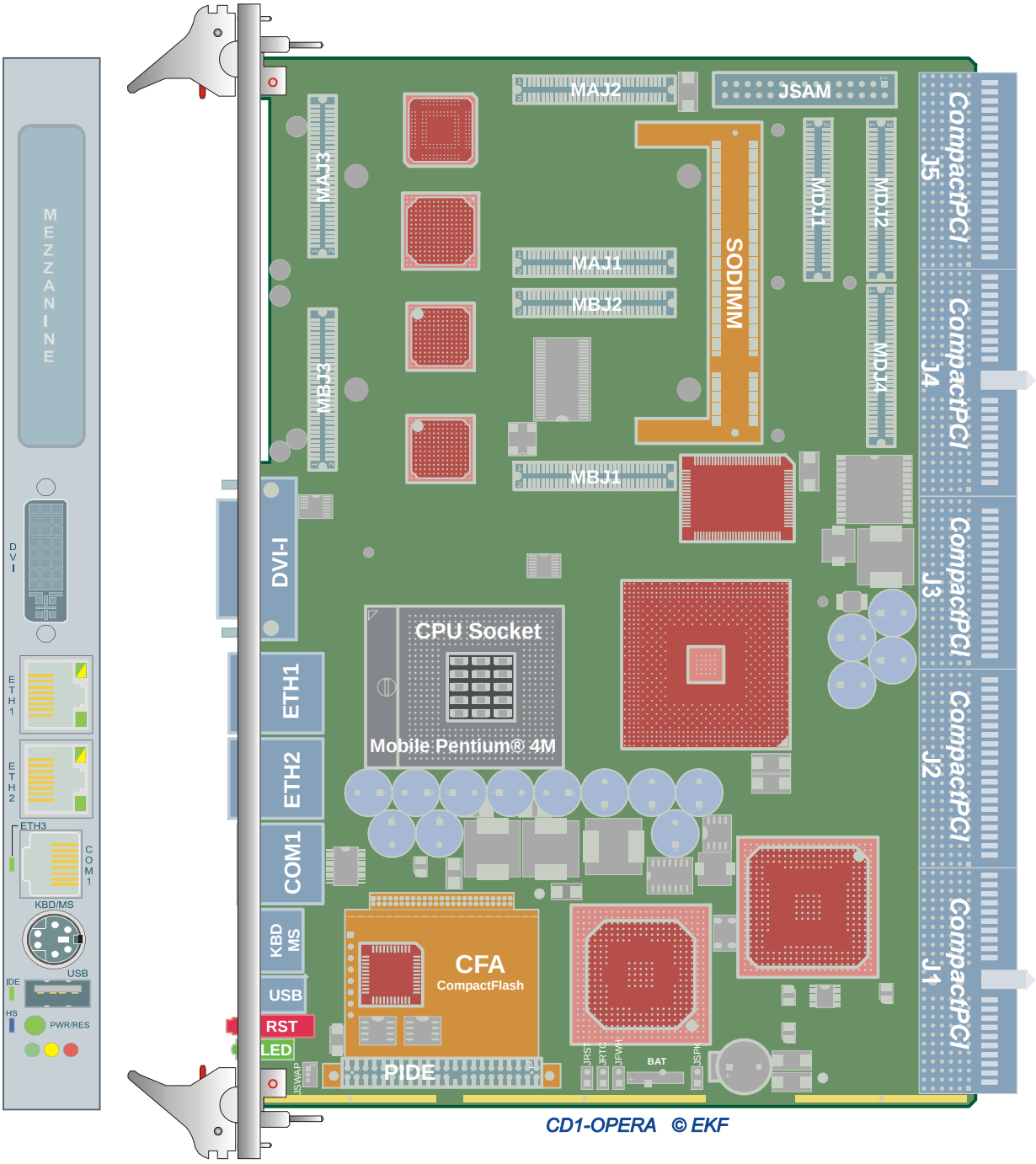
Top View Component Assembly CD1-OPERA



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Strapping Headers

Strapping Headers	
ISPCON	PLD Programming Connector (not stuffed)
JFWH	Firmware Hub ID Selector
JRST	*CompactPCI* Reset Selector (stuffed optionally)
JRTC	Reset Jumper CMOS Values (not stuffed)
JSWAP	Hot Swap Micro Switch Connector
JSPK	Speaker Connector

Connectors & Sockets

Connectors & Sockets	
CFA	CompactFlash ATA Socket (Secondary IDE Interface)
J1/J2	*CompactPCI* Bus 64-bit, 33/66MHz & PXI
J3	*CompactPCI* 2.16 Packet Switching Backplane Interface
J4/J5	*CompactPCI* Rear I/O Interface
JSAM	Multi-I/O Connector (COM2 (TTL), AC97, GPIO)
MAJ1-3	PC•MIP Slot A (stuffed optionally)
MBJ1-2	PC•MIP Slot B (stuffed optionally)
MDJ1/2/4	PMC Slot (stuffed optionally)
PIDE	Ultra ATA/100 Connector (Secondary IDE Interface)
PITP	CPU Debug Port
SODIMM	200-pin Memory Module DDR SDRAM PC2100

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Front Panel Elements

Front Panel Elements	
DVI-I	DVI-I receptacle, suitable for DVI digital flat panel displays and/or analog monitors
ETH1/ETH2	1000Base-TX/100Base-TX/10Base-T, RJ-45 Receptacle with integrated indicator LEDs
COM1	Serial Port COM1 (RS-232), RJ-45 Receptacle
KBD/MS	Keyboard/Mouse Interface, PS/2 style Mini-DIN Connector
USB	Universal Serial Bus 2.0 self powered root hub, Type A Receptacle
RST	Push-Button Switch with integrated indicator LED (power good)
LED	3 software programmable LEDs (green, yellow, red)
ETH3	Underfloor LED indicating Link/Activity on PICMG 2.16 Port
IDE	Underfloor LED indicating any IDE activity
HS	Underfloor Hot Swap LED

CD1-OPERA with on-Board Hard Disk Module

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Optional on-Board Hard Disk Module

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CD1-OPERA & CDX-RIO

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Microprocessor

The CD1-OPERA is designed to carry a 478-pin mPGA socketed Mobile Pentium® 4 Processor-M. These processors are also known as Northwood. The CD1 is not suitable for desktop mPGA478 Pentium®-4 processors. The table below lists typical processors available for the CD1-OPERA (there might be other resources not mentioned here). Please note: Use of any processor not supported can cause permanent damage to the processor and the CD1-OPERA!

Neither have all of the CPU types mentioned in the tables below been tested by EKF for use with the CD1-OPERA, nor does EKF claim that the entire range of processors is available for purchase. Instead, please refer to the EKF price list http://www.ekf.de/liste/liste_20.html for availability of the CD1-OPERA with particular processors (your individual request to sales@ekf.de is very welcome).

Please do not attempt to change or remove the installed processor by yourself. The CD1-OPERA is equipped with a passive heatsink, that is fixed by several screws, which need to be precisely adjusted in order achieve the optimum heat conduction. Furthermore, the heatsink is fixed with conductive pads and/or adhesion to the Northwood processor, which cannot be removed and renewed without suitable material and knowledge. If it is required to identify a particular processor, use suitable software instead, like Intels freely available Processor Frequency ID Utility.

Do not confuse the processor host bus frequency (FSB front side bus or PSB processor side bus) with the memory speed or the PCI clock, which are independent from each other. The processor signals its appropriate basic speed to the chipset, which is thereby adjusted automatically (no user interaction required). The internal CPU speed is achieved by multiplying the host bus frequency by a fixed value.

The CD1-OPERA is powered across the *CompactPCI* connectors J1/J2 (+3.3V, +5V). The processor core voltage is generated by a switched voltage regulator, sourced from the 5V plane. Any Northwood processor signals its required core voltage by 5 dedicated pins, hence there is no need (no choice) for user adjustment. Manipulation of these parameters (the euphemistic term 'tuning' is widely in use for that) may lead to unpredictable results.

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Pentium® 4 Processor-M Currently Supported (as of 09/2003)						
Processor	Speed Perf Mode/ Bat Mode	Voltage Perf Mode/ Bat Mode	Host Bus	L2 Cache	CPU ID	Stepping
Pentium 4-M	1.4/1.2GHz	1.3/1.2V	400MHz	512KB	0f24h	B0-Shrink
Pentium 4-M	1.5/1.2GHz	1.3/1.2V	400MHz	512KB	0f24h	B0-Shrink
Pentium 4-M	1.6/1.2GHz	1.3/1.2V	400MHz	512KB	0f24h 0f27h	B0-Shrink C1
Pentium 4-M [1)]	1.7/1.2GHz	1.3/1.2V	400MHz	512KB	0f24h 0f27h	B0-Shrink C1
Pentium 4-M	1.8/1.2GHz	1.3/1.2V	400MHz	512KB	0f24h 0f27h 0f29h	B0-Shrink C1 D1
Pentium 4-M	1.9/1.2GHz	1.3/1.2V	400MHz	512KB	0f24h 0f27h 0f29h	B0-Shrink C1 D1
Pentium 4-M	2.0/1.2GHz	1.3/1.2V	400MHz	512KB	0f24h 0f27h 0f29h	B0-Shrink C1 D1
Pentium 4-M [1)]	2.2/1.2GHz	1.3/1.2V	400MHz	512KB	0f27h 0f29h	C1 D1
Pentium 4-M	2.4/1.2GHz	1.3/1.2V	400MHz	512KB	0f27h 0f29h	C1 D1
Pentium 4-M	2.5/1.2GHz	1.3/1.2V	400MHz	512KB	0f27h 0f29h	C1 D1

[1)] following the Intel Embedded Roadmap, these processors are recommended for long time availability

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Thermal Considerations

In order to avoid malfunctioning of the CD1-OPERA, take care of appropriate cooling of the processor and system, e.g. by a cooling fan suitable to the maximum power consumption of the CPU chip actually in use. Please note, that the processors temperature is steadily measured by a special controller (MAX1617), attached to the onboard SMBus® (System Management Bus). The processor core (die) temperature is signalled by the forward voltage of a CPU integrated diode. A second diode internal to the MAX1617 allows for acquisition of the boards surface temperature. The programmable over-temperature alarm allows to trigger the SMBus alert line in order to avoid overheating. A suitable software to display both, the die temperature, as well as the board temperature, is MBM (Motherboard Monitor) for Windows (could be downloaded from the web) and LMSENSORS for Linux.

By default, the CD1-OPERA is equipped with a passive heatsink, that is used the cool the processor and also a part of the chipset. The heatsink is covering not only the processor chip itself but also major areas on the board, for an optimum thermal conduction. In addition, a forced vertical air flow trough the system enclosure (e.g. bottom mount fan unit) is strongly recommended. Be sure to thoroughly discuss your actual cooling needs with EKF. Generally, the faster the CPU speed the higher is its power consumption.

The maximum power consumption and operating temperature of a particular processor can be derived from the tables below. Fortunately, the power consumption is by far lower when executing typical Windows or Linux tasks. The heat dissipation increases especially when rendering software is executed, e.g. the Acrobat Distiller. EKF tests the CD1-OPERA by running proprietary Intel power tools for generating the maximum stress to the processor.

Pentium® 4 Processor-M Maximum Power Consumption and Die Temperature (09-2003)					
Speed/Voltage	Host Bus	L2 Cache	CPU ID	maximum Power	max. Die Temperature
1.2GHz/1.2V [1)]	400MHz	512KB	0f24h	20.8W	100˚C
1.4GHz/1.3V	400MHz	512KB	0f24h	25.8W	100˚C
1.5GHz/1.3V	400MHz	512KB	0f24h	26.9W	100˚C
1.6GHz/1.3V	400MHz	512KB	0f24h 0f27h	30.0W	100˚C
1.7GHz/1.3V	400MHz	512KB	0f24h 0f27h	30.0W	100˚C
1.8GHz/1.3V	400MHz	512KB	0f24h 0f27h 0f29h	30.0W	100˚C
1.9GHz/1.3V	400MHz	512KB	0f24h 0f27h 0f29h	32.0W	100˚C

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Pentium® 4 Processor-M Maximum Power Consumption and Die Temperature (09-2003)					
Speed/Voltage	Host Bus	L2 Cache	CPU ID	maximum Power	max. Die Temperature
2.0GHz/1.3V	400MHz	512KB	0f24h 0f27h 0f29h	32.0W	100˚C
2.2GHz/1.3V	400MHz	512KB	0f27h 0f29h	35.0W	100˚C
2.4GHz/1.3V	400MHz	512KB	0f27h 0f29h	35.0W	100˚C
2.5GHz/1.3V	400MHz	512KB	0f27h 0f29h	35.0W	100˚C

[1)] This is the so called "Battery Optimized" mode that the Northwood enters after system reset.

The mobile Northwood processor provides a few methods to reduce the power consumption. One is to let the processor in the "Battery Optimized" mode that it enters after a system reset. The BIOS provides a switch that controls whether the processor is brought to "Maximum Performance" mode during system startup.

Another way to reduce power consumption is to force the processor into the 'Throttle Mode'. This is achieved by actuating the 'Stop Clock' input of the CPU. A Throttle Mode of 50% e.g. means a duty cycle of 50% on the stop clock input. However, while saving considerable power consumption, the data throughput of the processor is also reduced. The mobile Northwood processor contains a thermal control circuit (TCC) that supports two modes of throttling: The automatic and the on-demand mode. When running in automatic mode the processor works full speed until the core temperature reaches a critical value. Then the processor is throttled by 30-50%. As soon as the high temperature situation disappears the throttling will be disabled and the processors runs at full speed again. The on-demand mode can be used to set fixed throttle values. All these features are controllable by BIOS menu entries.

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Main Memory

The CD1-OPERA is equipped with a socket for installing a single 200-pin SO-DIMM module (module height = 1.25 inch). Supported are unbuffered SODIMMs without ECC, according the PC1600 or PC2100 specification. Minimum memory size is 32MB; maximum memory size is 1024MB. Due to the video requirements of the i845G chipset, minimum memory for the Windows NT 4.0 and Windows 2000 operating system is 64MB (some of the system memory is dedicated to the graphics controller). The contents of the SPD eeprom is used by the BIOS at POST (Power-on Self Test) to program the memory controller within the chipset and is displayed on system start by the BIOS.

LAN Subsystem

The CD1-OPERA's LAN subsystem consists of 3 Intel 82540 Gigabit Ethernet controllers. Two of these are accessible via the front panel RJ-45 connectors, the 3rd is used for *CompactPCI* backplane packet switching (acc. PICMG Spec 2.16). The 82540 includes the following features:

- PCI bus mastering 32-bit, 33MHz
- 1000Base-Tx (Gigabit Ethernet), 100Base-TX (Fast Ethernet) and 10Base-T (Classic Ethernet) capability using a single RJ-45 connector
- half- or full-duplex operation
- IEEE 802.3µ Auto-Negotiation for the fastest available connection
- Jumperless configuration (complete software-configurable)

Two bicolour LEDs integrated in each of the RJ-45 connectors signal the LAN link, connection speed and activity status. A underfloor LED (located near the COM1 connector) flags the link and activity status for the backplane Ethernet interface.

The Intel 82540 Gigabit Ethernet PCI LAN software and drivers are available from Intel's World Wide Web site.

Enhanced IDE Interface

The EIDE interface handles the exchange of information between the processor and peripheral devices like hard disks, ATA CompactFlash cards and CD-ROM drives. The interface supports:

- Up to four ATA devices (including CompactFlash slot)
- PIO Mode 3/4, Ultra ATA/33, Ultra ATA/66, Ultra ATA/100
- Support for LS-120 drives

The primary IDE interface is routed to the *CompactPCI* J4 connector. A rear I/O adapter allows the connection of a master and a slave IDE device via a standard 40-pin flat ribbon cable (use special 80-pin cabling assembly for Ultra ATA/66 or /100 operation).

Optionally the primary IDE port is routed to the connector MDJ4 instead of J4 to support an on-board hard disk mounted on the PMC mezzanine slot. EKF offers a dedicated mounting kit that carries a 2.5" hard disk drive.

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The secondary IDE port is routed to the on-board 44-position header PIDE (2.0mm pitch), allowing master and slave device attached to one common flat ribbon cable (use special 80-pin cabling assembly for Ultra ATA/66 or /100 operation). This IDE interface is also routed to the CompactFlash Card Adapter socket CFA. Use this connector to attach a CompactFlash ATA style silicon disk, whenever a hard disk is not suitable for your system, or as an additional mass storage device.

Note: Either a CompactFlash Card or a flat ribbon cable on PIDE can be attached at the same time. If a CompactFlash Card and an external IDE device is needed, use the primary IDE port accessible via rear I/O.

An underfloor LED, situated in the front panel near the USB receptacle, signals disk activity status of the primary and the secondary IDE devices as well as the CompactFlash slot.

Graphics Subsystem

The graphics subsystem is part of the Intel i845G Graphic/Memory Controller Hub (GMCH), supporting the following features:

- 3-D Setup and Render Engine
- High Quality Texture Engine
- 3-D Graphics Rasterization Enhancements
- 2-D Graphics Hardware Acceleration
- Video DVD/PC-VCR
- Integrated 24-bit 350MHz RAMDAC
- DDC2B compliant

The CD1-OPERA is provided with the DVI-I graphics connector. This is both a digital and analog interface. Recent digital input flat-panel displays are already available with this connector style. Adapter cables can be used for converting to the 15-pin HD-SUB connector.

A special display transmitter chip is used for serializing/deserializing the differential DVI signals. The SiI 164 (Silicon Image) transmitter uses PanelLink® Digital technology to support displays ranging from VGA to SXGA resolutions (25-165Mpps) in a single link interface. It can be foreseen, that DVI will overcome the legacy analog and proprietary digital interfaces in the near future.

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Real-Time Clock

The CD1-OPERA has a time-of-day clock and 100-year calendar. A battery on the board keeps the clock current when the computer is turned off. The CD1-OPERA uses a Vanadium-Pentoxide-Lithium rechargeable battery, giving an autonomy of more than 80 days when fully loaded after 24 hours. The cell is free of memory effects and withstands deep discharging. Under normal conditions, replacement should be superfluous during lifetime of the board.

Universal Serial Bus (USB)

The CD1-OPERA is provided with three independent USB ports. A single USB 2.0 port is routed to a USB receptacle in the front panel. Any USB peripheral device (USB 1.1 or 2.0) can be attached directly to this connector. The front panel USB port can source up to 0.5A/5V and is protected by a self resetting, current limiting power switch against shortening.

To attach more devices, two further USB 2.0 ports are routed to the *CompactPCI* connector J4 and available via a rear I/O board.

PS/2 Keyboard/Mouse Interface

The CD1-OPERA offers a legacy PS/2 style keyboard and mouse port combined in a single mini-DIN connector. Split cables to attach both keyboard and mouse are available by EKF. The PS/2 interface is protected by a self resetting, current limiting power switch against shortening and can source up to 0.5A/5V.

Serial Interfaces

Two standard serial interfaces are available on the CD1-OPERA, both offering full modem support. One port (COM1) is accessible via a RJ-45 connector in the front panel (RS-232). Adapters to standard DSub-9M connectors are offered by EKF.

The 2nd port (COM2) is feed to the *CompactPCI* J4 connector for rear I/O as well as to the multi-I/O header JSAM. The usage of COM2 on J4 or JSAM is alternative. The interface for COM2 on JSAM is layed out in a manner that allows the selecting of different I/O standards (e.g. RS-232, RS-485, optical-isolated) by use of serial interface adapters (SA modules).

Parallel Interface

The CD1-OPERA provides a standard parallel port, e.g. for connecting printers, that is routed to the *CompactPCI* connector J4 for rear I/O connection.

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Floppy Disk Interface

Even if modern systems have replaced their legacy ports by USB or IDE, a standard 1.44MB floppy disk drive interface is still provided by the CD1-OPERA. The port is feed to the *CompactPCI* J4 connector, accessible via a rear I/O board.

Power Monitoring/Watchdog/Reset

The CD1-OPERA is provided with several circuits to monitor the various voltage planes (e.g. 3.3V, 5V, processor core voltage) and to generate a clean system reset on power up or malfunction. The MAX705 supervisor circuit is responsible for generating the reset signal. The manual push-button reset is passed through the MAX705 for appropriate pulse conditioning.

The manual reset push-button is placed in the front panel. The button is indent mounted behind the front and requires a tool, e.g. pen to be pressed, preventing from being inadvertently activated. The push-button reset signal is routed across a PLD (programmable logic device) and could be passivated on customers request.

The healthy state of the CD1-OPERA is signalled by the LED PWR integrated into the reset push-button. As soon as this LED lights up all power voltages are well and the reset signal is removed. This LED is also software programmable. See the section "PWR (Board Healthy) LED" how to do this.

Another feature is the watchdog function, which can be be programmed by software. The behaviour of the MAX705 watchdog is partially defined by the PLD, which controls whether the watchdog is activated. The related software (e.g. BIOS, application program) must trigger the watchdog by toggling the GPIO21 signal of the ICH4 (82801D).

The watchdog is in a passive state after a system reset. There is no need to trigger it at boot time. Once the GPIO21 of the ICH4 was pulsed the watchdog is activated. If the duration between two trigger pulses exceeds a period of 1000ms the watchdog timed out and a system reset is generated. The watchdog remains in the active state until the next system reset. There is no way to disable it once it was started.

Firmware Hub (Flash BIOS)

The BIOS is stored in a 82802AC compatible Firmware Hub (there are second sources available with deviant part numbers) with a capacity of 8Mbit. The CD1-OPERA offers two of these firmware hubs (FWHs) that can be accessed independently from each other. An FWH contains a nonvolatile memory core based on flash technology, allowing the BIOS to be upgraded.

The FWHs are soldered on the CD1-OPERA. They can be reprogrammed onboard by a DOS based tool. This program and the latest CD1-OPERA BIOS are available from the EKF website. Read carefully the enclosed instructions. If the programming procedure fails e.g. caused by a power failure, the CD1-OPERA may no more be operable. Since the CD1 offers 2 FWHs, a security copy in the 2nd FWH can be activated by the jumper JFWH in case of a failed BIOS update and the procedure may be repeated.

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Mezzanine Interfaces

To support the usage of PMC or PC•MIP mezzanine I/O modules, EKF offers two basic versions of the CD1-OPERA.

A single PMC module is mountable e.g. on the CD1-1-OPERA. The PMC slot on the CD1 supports a 32-bit/33MHz PCI interface with $V_{I/O}$=3.3V. The modules rear I/O is wired to the *CompactPCI* connector J5. Alternatively I/O can be obtained via the front panel connector of the module (if any).

Up to two single sized or one double sized PC•MIP module may be carried by the CD1-2-OPERA. One of these PC•MIP slots supports rear I/O as well as front I/O modules (type I and II), the other slot is applicable for front I/O modules (type II) only. The rear I/O's are routed to the *CompactPCI* connector J5.

Alternatively the mezzanine slots are usable for an on-board hard disk drive. EKF offers a dedicated mounting kit that carries a 2.5" hard disk drive.

PWR (Board Healthy) LED

The CD1-OPERA offers a software programmable LED located in the reset push-button. After system reset, this LED defaults to signal the board healthy. By the first setting of the GPIO20 of the ICH4 this LED changes its function and is then controlled only by the level of the GPIO20 pin. Setting this pin to 1 will switch on the LED.

The PWR LED remains in the programmable state until the next system reset.

General Purpose LEDs

Three further, user programmable LEDs (green, yellow and red) can be also observed from the front panel (placed between the reset push-button and the front panel ejector). The status of these LEDs is controlled by GPIOs of the ICH4 as listed below:

LED	ICH4 Control Pin
green	GPIO25
yellow	GPIO27
red	GPIO28

Note, that an LED illuminates if the level of the corresponding GPIO is low.

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CompactPCI Bridge HB6

To create a data path to the *CompactPCI* backplane the CD1-OPERA is equipped with the universal PCI-To-PCI bridge HB6 manufactured by HiNT. Advantages of this universal bridge are its possible operation as either transparent or non-transparent bridge and the hot swap support according the PICMG 2.1 R2.0 *Hot Swap Specification*. The HB6's mode of operation is chosen by the level of the *CompactPCI* signal SYSEN# located on connector J2 pin C2. SYSEN# is low on the system controller slot only, bringing the HB6 into transparent mode. On all other slots the HB6 works as non-transparent bridge. Nevertheless only the system slot versions of the CD1 (see section "Ordering Information") will work proper in the system slot because it will provide all the necessary pull-up resistors required by the *CompactPCI* specification.

Transparent Mode

As mentioned above the system controller mode versions of CD1 use the HB6 as a standard transparent PCI bridge. The HB6 keeps a 64 bit width data bus and operates at 33MHz (66MHz available on request). It provides 7 pairs of bus request/bus grant lines for supporting *CompactPCI* backplanes with up to 8 slots.

The initializations necessary in transparent mode are done completely by the BIOS. Once the HB6 is configured, any device on a peripheral board is seen like a device located within the own address space. On operating system level there is no need for any software management. No changes are necessary to the corresponding software device drivers.

Non-Transparent Mode

Unlike the VMEbus, the *CompactPCI* bus was not designed for multiple processor boards which share a common backplane. Instead one system slot controller (CPU board) has been defined; all other card slots are reserved for peripheral I/O boards. In order to achieve multi-processing, additional CPU boards on the *CompactPCI* bus must hide themselves behind a non-transparent PCI bridge (NTB). This is what mainly distinguishes the CD1 peripheral version from the system slot controller version.

On peripheral versions of the CD1 the HB6 is working as non-transparent PCI bridge, acting as a gateway to the intelligent subsystem. It allows the local processor to independently configure and control the local subsystem. The processor domain on the primary interface of the HB6 is also referred to as the host domain, and its processor is the host processor. The secondary bus interfaces to the local domain and the local processor. Special features include support of independent primary and secondary address spaces, and address translation between the primary (host) and secondary (local) domains.

The NTB forwards transactions between the primary and secondary PCI buses when falling in an appropriate address window as done by a transparent bridge. In contrast to the transparent mode, an address of a forwarded transaction is translated from a system address to a local address, or vice versa. This mechanism allows the NTB to hide subsystem resources from the host processor and to resolve any resource conflicts that may exist between the host and local subsystems.

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In non-transparent mode the HB6 uses a Type 0 configuration header, which presents the entire subsystem as a single device to the host processor. This allows loading of a single device driver for the entire subsystem. Since the HB6 uses a Type 0 configuration header, it does not require hierarchical PCI-to-PCI bridge configuration code.

Hot Swap Function

The CD1-OPERA is a hot swapable board that fulfils the "Full Hot Swap" criteria of the *CompactPCI* PICMG 2.1 R2.0 Hot Swap Specification. The peripheral versions of the board (e.g. CD1-A-OPERA, see section "Ordering Information") can be inserted in or removed from a living system rack without influencing other parts within the system. The hot swap of a system slot CD1 is principally possible, but makes less sense since without system controller no peripheral board is able to run. The CD1 is also capable to recognize the hot swap of peripheral boards and to start software that is doing any necessary system reconfiguration when working as system controller unit.

Hot Swap Power Controller

The CD1 uses a LTC1646 hot swap power controller. The main task of this device is a controlled switching of the board power supplies. On board insertion the various power planes on the board (3.3V, 5V, ±12V) are ramped up slowly to avoid too large voltage drops within the system. When all voltages have reached their nominal values the controller asserts the *CompactPCI* signal HEALTHY# (connector J1 pin B4). Electronic circuit breakers protect +3.3V and +5V against overcurrent fault conditions. As soon as the current on these supplies exceed a value of 11A, the power of all supplies (including ±12V) are switched off and the fault is flagged to the system by deasserting the HEALTHY# signal.

Hot Swap Detection (ENUM#)

To support full hot swap the *CompactPCI* hot swap specification added the signal ENUM# to the PCI bus to inform the system controller for hot swap events. This signal is routed to the GPIO0 of the ICH4 on the CD1-OPERA. A System Management Interrupt (SMI) can be requested if ENUM# changes by insertion or removal of a board. When working in peripheral mode, the CD1 drives this signal to flag its hot swap events.

Blue Hot Swap LED

The full hot swap capability also includes the control of a blue LED (an underfloor LED marked as HS and placed in the front panel near the reset push-button), that indicates when board extraction is permitted. A micro switch in one of the front panel ejectors signals when a board extraction event takes place. This micro switch is connected via the 3-pin header JSWAP.

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Power Supply Status (DEG#, FAL#)

Power supply failures may be detected before the system crashes down by monitoring the signals DEG# or FAL#. These low active lines are additions of the *CompactPCI* specification and may be driven by the power supply. DEG# signals the degrading of the supply voltages, FAL# there possible failure. On the CD1-OPERA the signal FAL# is routed to the GPIO6 and DEG# to the GPIO7 of the ICH4.

PXI Trigger Signals

TBD

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Installing and Replacing Components

Before You Begin

Warnings

The procedures in this chapter assume familiarity with the general terminology associated with industrial electronics and with safety practices and regulatory compliance required for using and modifying electronic equipment. Disconnect the system from any telecommunication links, networks or modems before performing any of the procedures described in this chapter. Failure to disconnect telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage. Some parts of the system can continue to operate even though the power switch is in its off state.

Do not expose the board to fire. Battery cells and other components could explode and cause personal injury.

Caution

Electrostatic discharge (ESD) can damage components. Perform the procedures described in this chapter only at an ESD workstation. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis or board front panel. Store the board only in its original ESD protected packaging. Retain the original packaging (antistatic bag and antistatic box) in case of returning the board to EKF for rapair.

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Installing the Board

Board insertion may be done in a running *CompactPCI* system. Typically you will perform the following steps:

- Attach your antistatic wrist strap to a metallic part of the system.
- Remove the board packaging, be sure to touch the board only at the front panel.
- Identify the related *CompactPCI* slot (peripheral slot for I/O boards, system slot for CPU boards, with the system slot typically most right or most left to the backplane).
- Insert board carefully and push it slowly over the guide rails, but do not contact it with any backplane connectors. Be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels.
- Attach any necessary cabling to the board's front panel and onboard connectors.
- Press the board into the backplane connectors by the ejector lever(s) until the lever locks. The blue hot swap LED illuminates during this process.
- Retain original packaging in case of return.

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Removing the Board

Board extraction may be done from a running *CompactPCI* system. Typically you will perform the following steps:

- Attach your antistatic wrist strap to a metallic part of the system.
- Identify the board, be sure to touch the board only at the front panel.
- Unlock the ejector lever.
- As soon as the blue hot swap LED illuminates, activate the ejector lever to pull the *CompactPCI* connectors out of the backplane. [1)]
- Remove any front panel and onboard cabling assembly.
- Remove the board carefully. Be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels.
- Store board in the original packaging, do not touch any components, hold the board at the front panel only.

Note [1)]:
To wait for the LED to illuminate is not necessary when extracting the board from a powerless system.

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EMC Recommendations

CE

In order to comply with the CE regulations for EMC, it is mandatory to observe the following rules:

- The chassis or rack including other boards in use must comply entirely with CE
- Close all board slots not in use with a blind front panel
- Front panels must be fastened by built-in screws
- Cover any unused front panel mounted connector with a shielding cap
- External communications cable assemblies must be shielded (shield connected only at one end of the cable)
- Use ferrite beads for cabling wherever appropriate
- Some connectors may require additional isolating parts

Recommended Accessories		
Blind CPCI Front Panels	EKF Elektronik	Widths currently available (1HP=5.08mm): with handle 4HP/8HP without handle 2HP/4HP/8HP/10HP/12HP
Ferrit Bead Filters	ARP Datacom, 63115 Dietzenbach	Ordering No. 102 820 (cable diameter 6.5mm) 102 821 (cable diameter 10.0mm) 102 822 (cable diameter 13.0mm)
Metal Shielding Caps	Conec-Polytronic, 59557 Lippstadt	Ordering No. CDFA 09 165 X 13129 X (DB9) CDSFA 15 165 X 12979 X (DB15) CDSFA 25 165 X 12989 X (DB25)

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Installing or Replacing the Processor

Note: If you decide to install a processor on your own, observe the precautions in 'Before You Begin'

As default, the CD1-OPERA comes fully equipped and tested with a processor. So normally there should be no need to install a processor.

Although the CD1-OPERA features a ZIF (zero insertion force) socket for the processor we suggest that you install or replace the processor only if you own an ESD workstation.

Before the processor can be replaced, you would have to remove the passive heatsink, which is fitted by screws to the board and attached by conductive pads and/or adhesion to the processor. Special handling is required to remove the heatsink and to re-install it afterwards, including renewing the conductive adhesion and adjustment of the mounting screws.

Conclusion: Do not attempt to replace the processor by yourself, unless you are an absolute professional. Instead, send in the board to EKF.

Installing or Replacing the Memory Module

Note: If you decide to replace the memory, observe the precautions in 'Before You Begin'

By default, the CD1-OPERA comes fully equipped and tested with a DDR SDRAM memory module. So normally there should be no need to install a memory module.

The CD1-OPERA requires a PC1600/DDR200 (100MHz) or PC2100/DDR266 (133MHz) DDR SDRAM SO-DIMM module. It is highly recommended that Serial Presence Detect (SPD) SO-DIMMs be used, since this allows the chipset to accurately configure the memory settings for optimum performance. If non-SPD memory is installed, the BIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted.

A replacement memory module must match the 200-pin SO-DIMM form factor (known from Notebook PCs), 2.5V, 100MHz or 133MHz, unbuffered, non-ECC style. Suitable modules are available up to 1GB. The 845GMCH supports modules of up to a maximum of 13 address lines (A0...A12). Memory modules organized by more than13 address lines are not suitable.

Before the memory module can be replaced, a possibly mounted mezzanine module must be removed from the board. See section below how to do this.

Conclusion: Replacement of a memory module is easy, but unnecessary in most cases.

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Installing PC•MIP Modules

Note: If you want to mount a mezzanine module, observe the precautions in 'Before You Begin'

To simplify the installation and removing of a module PC•MIP uses an injector/ejector system. This consists of two mounting standoffs on the CD1-OPERA and two captive screws located at each end of the module. This construction offers the advantage, that the screws are used to fasten the module on the carrier board and in addition that the screws push the module out of the connectors when unfasten the connection.

To install a module put the module loose on the PC•MIP slot and fix the two screws by turning them clockwise. This will pull the module connectors in the corresponding receptacle of the CD1 and fasten it. Note, that PC•MIP slot A is capable to carry type I and type II modules, while slot B only supports type II modules (no rear I/O).

A PC•MIP module is removed by turning the ejector screws counterclockwise. This will pushing the module out of the connectors until it could be taken off.

Installing a PMC Module

Note: If you want to mount a mezzanine module, observe the precautions in 'Before You Begin'

A PMC module is fasten on the CD1-OPERA via 4 screws, two are screwed on mounting standoffs on the top side of the CD1 and two screws are located on the solder side of the CD1 near the front panel.

To install a module put the module loose on the PMC slot and fix the two top side screws by turning them clockwise. This will pull the module connectors in the corresponding receptacle of the CD1 and fasten it. Turn the CD1 and mount the two solder side screws.

Remove a module by turning first the solder side and then the top side screws counterclockwise.

Replacement of the Battery

When your system is turned off, a battery maintains the current time-of-day clock and the values in CMOS RAM current. The battery is rechargeable und should last during the lifetime of the CD1-OPERA. For replacement, the old battery must be desoldered, and the new one soldered. Observe the cell polarization. We suggest that you send back the board to EKF for battery replacement.

Warning

Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type. Do not expose a battery to fire.

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Technical Reference

Local PCI Devices

The following table shows the on-board PCI devices and their location within the PCI configuration space. These devices consist of the three Ethernet controllers, the two PCI-To-PCI Bridges, the PXI controller and several devices within the i845G chip set.

Bus Number	Device Number	Function Number	Vendor ID	Device ID	Description
0	0	0	0x8086	0x2560	Host Bridge
0	2	0	0x8086	0x2562	VGA Display
0	29	0	0x8086	0x24C2	USB UHCI Controller #1
0	29	1	0x8086	0x24C4	USB UHCI Controller #2
0	29	2	0x8086	0x24C7	USB UHCI Controller #3
0	29	7	0x8086	0x24CD	USB 2.0 EHCI Controller
0	30	0	0x8086	0x244E	Hub Interface Bridge
0	31	0	0x8086	0x24C0	LPC Bridge
0	31	1	0x8086	0x24CB	IDE Controller
0	31	3	0x8086	0x24C3	SMB Controller
0	31	5	0x8086	0x24C5	AC'97 Audio Controller
0	31	6	0x8086	0x24C6	AC'97 Modem Controller
2	0	0	TBD	TBD	PCI-To-PXI Bridge
2	1	0	0x8086	0x100E	Ethernet Controller #1
2	2	0	0x8086	0x100E	Ethernet Controller #2
2	3	0	0x8086	0x100E	Ethernet Controller #3
2	4	0	0x3388	0x0020 [1)] 0x0021 [2)]	PCI-To-PCI Bridge (CPCI)
2	5	0	0x104C	0xAC28	PCI-To-PCI Bridge (Mezzanines)

Notes:
[1)] When working as transparent PCI bridge (system controller versions of CD1)
[2)] When working as non-transparent PCI bridge (peripheral versions of CD1)

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Local SMB Devices

The CD1-OPERA contains a few devices that are reachable via the System Management Bus (SMB). These are the clock generation chip, the SPD EEPROM on the SO-DIMM memory module, the three Ethernet controllers and a CPU temperature controlling device in particular.

Other devices could be connected to the SMB via the *CompactPCI* signals IPMB SCL (J1 B17) and IPMB SDA (J1 C17). This interface is wired via a switch to the SMBus which is controlled by GPIO24 of the ICH4. A low level on this pin isolates the SMB signals from the *CompactPCI*. A menu item in the BIOS allows to control the switch behaviour.

Address	Description
0x30	CPU Temperature Sensor MAX 1617
0xA0	SPD of SO-DIMM
0xD2	Main Clock Generation

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Interrupt Mapping

Many devices on the CD1-OPERA are capable to request processor interrupts. The ICH4 provides 10 interrupt lines and supports also the serialized interrupt protocol SERIRQ. The following table show the mapping of the various interrupt requesters to the IRQ inputs of the ICH4:

Interrupt Input ICH4	Interrupt Requester
PIRQ A#	*CompactPCI* INTA# PCMIP Slot A INTB#, Slot B INTC# PMC INTD#
PIRQ B#	ETH3 (PICMG 2.16)
PIRQ C#	*CompactPCI* INTB# PCMIP Slot A INTC#, Slot B INTD# PMC INTA#
PIRQ D#	PCI-PCI Bridge (CPCI) [1)]
PIRQ E#	ETH1, PCI-PXI Bridge (PLD2)
PIRQ F#	*CompactPCI* INTC# PCMIP Slot A INTD#, Slot B INTA# PMC INTB#
PIRQ G#	CompactPCI INTD# PCMIP Slot A INTA#, Slot B INTB# PMC INTC#
PIRQ H#	ETH2
IRQ14	Primary IDE *CompactPCI* INTP [2)]
IRQ15	Secondary IDE *CompactPCI* INTS [3)]
SERIRQ	Super I/O *CompactPCI* INTS [4)] PMC MDJ2 Pin 9 [4)]

Notes:
[1)] Only for CD1 in peripheral mode (see section "Ordering Information")
[2)] A switch controlled by GPIO0 of the CPCI brigde connects INTP to IRQ14 (logical 1: switch on)
[3)] A switch controlled by GPIO1 of the CPCI brigde connects INTS to IRQ15 (logical 1: switch on)
[4)] A switch controlled by GPIO2 of the CPCI brigde connects this pin to SERIRQ (logical 1: switch on)

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PXI-To-PCI Bridge (PLD2)

The PXI-To-PCI bridge on the CD1-OPERA is realized in a programmable logic device (PLD2). The device actual used is an EP1K30 manufactured by Altera. Since this PLD is RAM based it must be loaded with a logic pattern after power up. To do this download PLD2 is interfaced to some GPIOs of the ICH4:

ICH4 Control	PLD2 Signal	Direction
GPIO23	CONFIG#	to PLD2
GPIO37	STATUS#	to ICH4
GPIO38	CONF_DONE	to ICH4
GPIO39	DCLK	to PLD2
GPIO40	DATA	to PLD2

Beside the PXI function PLD2 features also 16 GPIOs routed to the multi I/O header JSAM and to the *CompactPCI* rear I/O connector J4. Direction and level of these GPIOs are controlled by registers within PLD2.

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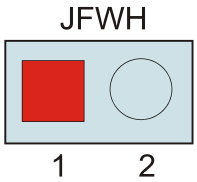
Configuration Jumpers

Firmware Hub ID Selection (JFWH)

The CD1-OPERA offers two firmware hubs FWH1 and FWH2 containing e.g. the BIOS boot code. They can be used independent from each other and will be distinguished by an identifier code. The two FWHs are assigned to the IDs #0 and #1. The processor always executes its first instructions after a system reset from FWH #0. The jumper JFWH serves the purpose to swap the ID numbers assigned to the FWHs thus allowing the processor to start execution from the other FWH.

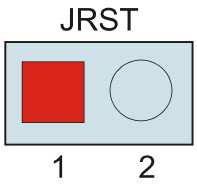


JFWH	FHW1 ID	FWH2 ID	Boot Device
Jumper OFF	#0	#1	FWH1
Jumper ON [1)]	#1	#0	FWH2

Note:
[1)] This setting is the factory default.

CompactPCI Reset Behaviour (JRST)

The jumper JRST is mounted on the peripheral versions of CD1 only (see section "Ordering Information"). It is used to control the behaviour of the board when the *CompactPCI* system reset signal becomes active.



JRST	Function
Jumper OFF	No local reset performed on CPCI system reset
Jumper ON [1)]	CPCI system reset also activates local reset

Note:
[1)] This setting is the factory default.

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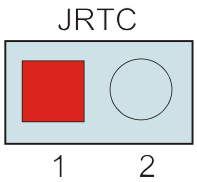
Reset Jumper CMOS Values (JRTC)

The jumper JRTC is used to bring the contents of the battery backed CMOS RAM to a default state. The BIOS uses the CMOS to store configuration values, e.g. the actual boot devices.

To reset the CMOS RAM the board must be removed from the system rack. Short-circuit the pins of JRTC for about 1 sec. After that reinstall the board to the system and switch on the power. It is important to accomplish the CMOS reset while the board has no power.



JRTC	Function
Jumper OFF [1)]	No CMOS reset performed
Jumper ON	CMOS reset performed

Note:
[1)] This setting is the factory default.

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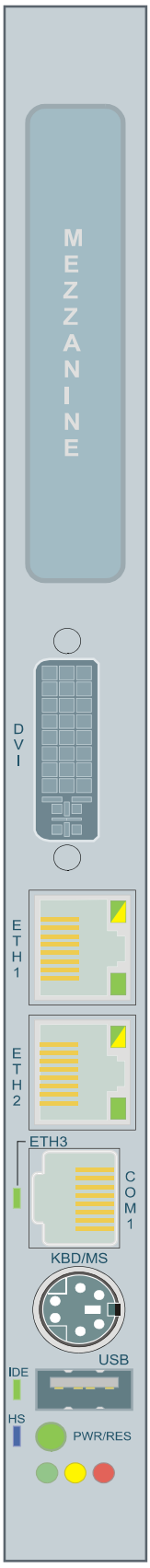
Connectors

Front Panel Connectors



CD1-OPERA Front Panel Elements

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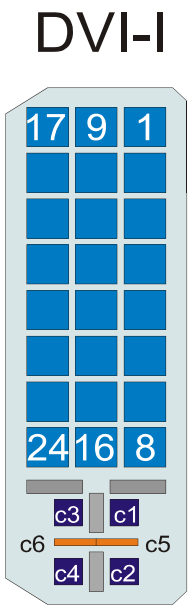
Video Monitor Connector DVI-I

DVI-I					
17	tx0-	9	tx1-	1	tx2-
18	tx0+	10	tx1+	2	tx2+
19	GND	11	GND	3	GND
20		12		4	
21		13		5	
22	GND	14	ddcpow	6	ddcl
23	txc+	15	GND	7	ddca
24	txc-	16	dvihp	8	vsync

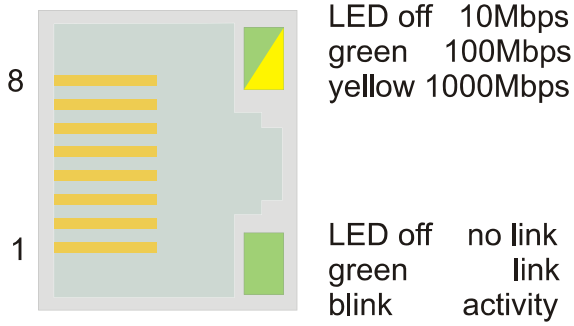
c3	blue	c1	red
c6	GND	c5	GND
c4	hsync	c2	green



For attachment of an ordinary analog RGB monitor to the DVI receptacle, there are both adapters and also adapter cables available from DVI-I to the HD-SUB15 connector. Attachment of digital monitors (flat panel displays) should be done by means of a DVI to DVI cable (single link style cable is sufficient).

Ethernet Connectors ETH1, ETH2 (RJ-45)

ETH1/ETH2 (RJ-45)	
MDX0+	1
MDX0-	2
MDX1+	3
MDX2+	4
MDX2-	5
MDX1-	6
MDX3+	7
MDX3-	8



The upper green/yellow dual-LED signals 1Gbit/s when lit yellow, 100Mbit/s when lit green, and 10Mbit/s when off. The lower green LED indicates LINK established when continuously on, and data transfer (activity) when blinking. If the lower green LED is permanently off, no LINK is established.

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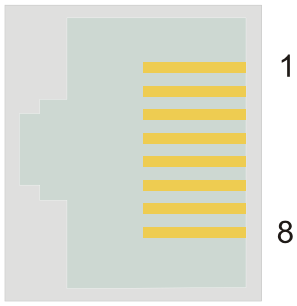
COM1 Connector (RJ-45)

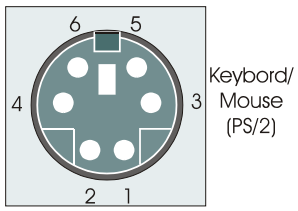
COM1 (RJ-45)			
1	Data Set Ready	DSR	Input
2	Data Carrier Detect	DCD	Input
3	Data Terminal Ready	DTR	Output
4	Ground	GND	
5	Receive Data#	RXD#	Input
6	Transmit Data#	TXD#	Output
7	Clear To Send	CTS	Input
8	Request To Send	RTS	Output



EKF offers adapter cables to transit from the RJ-45 to the standard DSub-9M connector.

Keyboard/Mouse Connector KBD/MS (PS/2)

1	Keyboard Data
2	Mouse Data
3	GND
4	+5V (limited to 0.5A)
5	Keyboard Clock
6	Mouse Clock



The PS/2 style Mini-DIN connector marked as KBD/MS provides a combine interface for both keyboard and mouse. A split cable is available by EKF support both devices simultanous. If a mouse is not required a keyboard may be attached directly to KBD/MS. The exclusive use of a mouse without a keyboard requires a cross-over adapter to match the pinning of KBD/MS on the CD1.

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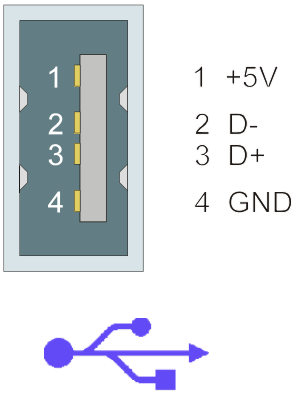
USB Connector

1	+5V (limited to 0.5A)
2	USB Data 0 (1) NEG
3	USB Data 0 (1) POS
4	GND



The connector is an USB A-style receptacle. Use any common USB cable for attachment of USB devices. The board is protected against devices with high power-on current or short circuit conditions across the USB cable by an electronic switch, which limits the maximum USB supply current to 0.5A nominal.

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Internal Connectors

Multi I/O Connector (JSAM)

JSAM						
COM2	Ground	GND	1	2	+5V	Power
	Transmit Data	TXD	3	4	RXD	Receive Data
	Data Terminal Ready#	DTR#	5	6	RTS#	Request To Send#
	Data Set Ready#	DSR#	7	8	CTS#	Clear To Send#
	Data Carrier Detect	DCD#	9	10	NC	No Connection
AC'97	Ground	GND	11	12	+5V	Power
	Serial Data Out	SDOUT	13	14	SDIN0	Serial Data In #0
	Codec Reset	RST#	15	16	SYNC	Codec Synchronize
	Serial Data Clock	BITCLK	17	18	SDIN1	Serial Data In #1
	Speaker	SPK	19	20	NC	No Connection
GPIO	Ground	GND	21	22	+5V	Power
	General Purpose I/O	GPIO0	23	24	GPIO1	General Purpose I/O
	General Purpose I/O	GPIO2	25	26	GPIO3	General Purpose I/O
	General Purpose I/O	GPIO4	23	24	GPIO5	General Purpose I/O
	General Purpose I/O	GPIO6	25	26	GPIO7	General Purpose I/O

The header JSAM consists of the three sections COM2, AC'97 and GPIO. Each section has its own power and ground pins to supply external connected devices.

Warning: Neither of the +5V pins is protected directly against a short circuit! In case of an overcurrent situation the hot swap controller circuit on the CD1-OPERA will limit the current and switching off any supply voltage immediately.

The 1st section of JSAM offers the serial port COM2. It is wired to connect standard serial adapter (SA) modules via a simple flat ribbon cable. Ask EKF for the different SA modules available. Since this serial port is routed to the *CompactPCI* rear I/O connector J5 also only one of these interfaces should be used.

The 2nd section of JSAM may be used to connect the AC'97 interface of the CD1 to an external Codec. Ask EKF for a special SA module supporting sound via AC'97.

The last section contains 8 simple general purpose I/O signals, that offer TTL level signaling (5V-proof). The direction and settings of the I/Os are controllable by registers within the PCI-PXI-bridge. On request these signals may fulfill more complex tasks than GPIO's like a 3rd serial port. Ask EKF for special programming within the PCI-PXI-Brigde.

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ATA/IDE Header (PIDE)

PIDE			
RESET#	1	2	GND
D07	3	4	D08
D06	5	6	D09
D05	7	8	D10
D04	9	10	D11
D03	11	12	D12
D02	13	14	D13
D01	15	16	D14
D00	17	18	D15
GND	19	20	KEY
DREQ	21	22	GND
IOW#	23	24	GND
IOR#	25	26	GND
IORDY	27	28	GND
DACK#	29	30	GND
INT (IRQ 15)	31	32	NC
A01	33	34	PDIAG
A00	35	36	A02
CS0#	37	38	CS1#
IDEACT#	39	40	GND
+5V	41	42	+5V
GND	43	44	NC

PIDE provides the secondary IDE port. This IDE port is shared with the CompactFlash slot (see section below). IDE drives may get their supply directly from the power supply pins of PIDE.

Warning: Neither of the +5V pins is protected directly against a short circuit! In case of an overcurrent situation the hot swap controller circuit on the CD1-OPERA will limit the current and switching off any supply voltage immediately.

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ATA CompactFlash Socket (CFA)

CompactFlash Socket CFA (True IDE Mode)			
CD1#	26	1	GND
D11	27	2	D03
D12	28	3	D04
D13	29	4	D05
D14	30	5	D06
D15	31	6	D07
CS1#	32	7	CS0#
VS1# (10k PU)	33	8	A10 (GND)
IORD#	34	9	ATA_SEL# (GND)
IORW#	35	10	A09 (GND)
WE# (Vcc)	36	11	A08 (GND)
INTRQ (IRQ15)	37	12	A07 (GND)
V_{CC} (+3.3V)	38	13	V_{CC} (+3.3V)
CSEL# (GND)	39	14	A06 (GND)
VS2# (10k PU)	40	15	A05 (GND)
RESET#	41	16	A04 (GND)
IORDY	42	17	A03 (GND)
INPACK#	43	18	A02
REG# (Vcc)	44	19	A01
DASP#	45	20	A00
PDIAG#	46	21	D00
D08	47	22	D01
D09	48	23	D02
D10	49	24	*IOCS16#*
GND	50	25	*CD2#*

pin positions printed italic/ coloured gray - not connected on CD1-OPERA

The CompactFlash specification 1.4 describes three different operating modes. The CD1-OPERA supports the True IDE mode only. Any CompactFlash storage card is required to support the True IDE mode.

The CompactFlash socket on the CD1 is connected to the secondary IDE port. The CFA shares this IDE port with that routed to the header PIDE (see section above).

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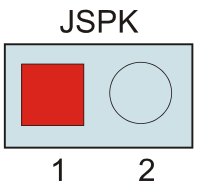
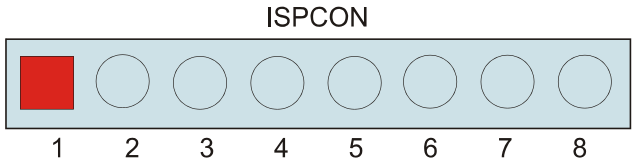
Speaker Header (JSPK)



1 +5V
2 Speaker

Warning: The +5V pin is not directly protected against a short circuit! The JSPK connector should be used exclusively for direct attachment of a dynamic speaker device. When connecting to the input of a sound card, most likely a short-circuit situation will occur between the +5V pin of the JSPK connector and the GND pin of the audio-card input, which could cause permanent damage to the audio board. A workaround to this would be to place a 1k resistor across pin 1 and pin 2 of the JSPK connector, and strapping a single wire cable from JSPK pin 2 to the audio input.

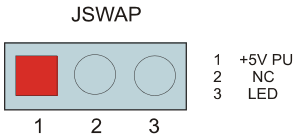
PLD Programming Header (ISPCON)



1 +5V
2 serial data out
3 serial data in
4 ispGAL enable
5 NC
6 mode
7 GND
8 serial clock

Note: The ISPCON is normally not stuffed. Its footprint is situated at the bottom side of the board.

Hot Swap Micro Switch Pin Row (JSWAP)



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Processor Debug Header (PITP)

PITP	
1	TDI
2	TMS
3	TRST#
4	NC
5	TCK
6	NC
7	TDO
8	BCLKN
9	BCLKP
10	GND
11	FBO
12	RST#
13	BPM5#
14	GND
15	BPM4#
16	GND
17	BPM3#
18	GND
19	BPM2#
20	GND
21	BPM1#
22	GND
23	BPM0#
24	DBA#
25	DBR#
26	VTAP
27/28	V_{TT}

Note: The Debug Header is placed at the bottom side of the board.

PC•MIP Slot MAJ1/MBJ1

MAJ1/MBJ1	Signal Name	Signal Name	MAJ1/MBJ1
1	*Reserved*	*Reserved*	2
3	*Reserved*	*Reserved*	4
5	-12V	*TRST#*	6
7	*TCK*	+12V	8
9	GND	*TMS*	10
11	*TDO*	*TDI*	12
13	+5V	+5V	14
15	+5V	INTD#/INTC# [1)]	16
17	INTA#/INTD# [1)]	INTB#/INTA# [1)]	18
19	INTC#/INTB# [1)]	+5V	20
21	*PRSNT1#*	*Reserved*	22
23	*Reserved*	+3.3V	24
25	*PRSNT2#*	*Reserved*	26
27	GND	GND	28
29	*Reserved*	*Reserved*	30
31	GND	RST#	32
33	CLK	+3.3V	34
35	GND	GNT#	36
37	REQ#	GND	38
39	+3.3V	*Reserved*	40
41	AD31	AD30	42
43	AD29	+3.3V	44
45	GND	AD28	46
47	AD27	AD26	48
49	AD25	GND	50
51	+3.3V	AD24	52
53	C/BE3#	IDSEL [2)]	54
55	AD23	+3.3V	56
57	GND	AD22	58
59	AD21	AD20	60
61	AD19	GND	62
63	+3.3V	AD18	64

pin positions printed italic/coloured brown: reserved by specification and not connected
pin positions printed italic/coloured blue: not connected on CD1-OPERA

Notes:
[1)] This pin position is showing the actual interrupt assignment for Slot A respective Slot B.
[2)] IDSEL is assigned to AD31 for Slot A and to AD30 for Slot B.

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PC•MIP Slot MAJ2/MBJ2

MAJ2/MBJ2	Signal Name	Signal Name	MAJ2/MBJ2
1	*Reserved*	*Reserved*	2
3	*Reserved*	*Reserved*	4
5	+5V	+5V	6
7	+5V	+5V	8
9	REQ64# [1)]	ACK64# [1)]	10
11	+3.3V	+3.3V	12
13	AD00	AD01	14
15	AD02	GND	16
17	GND	AD03	18
19	AD04	AD05	20
21	AD06	+3.3V	22
23	+3.3V	AD07	24
25	C/BE0#	AD08	26
27	GND	GND	28
29	AD09	*M66EN*	30
31	GND	AD10	32
33	AD11	AD12	34
35	AD13	GND	36
37	+3.3V	AD14	38
39	AD15	C/BE1#	40
41	PAR	+3.3V	42
43	GND	SERR#	44
45	*SBO#*	+3.3V	46
47	*SDONE*	PERR#	48
49	+3.3V	LOCK#	50
51	STOP#	GND	52
53	GND	DEVSEL#	54
55	TRDY#	+3.3V	56
57	GND	IRDY#	58
59	FRAME#	GND	60
61	+3.3V	C/BE2#	62
63	AD16	AD17	64

pin positions printed italic/coloured brown: reserved by specification and not connected
pin positions printed italic/coloured blue: not connected on CD1-OPERA

Notes:
[1)] This pin position is pulled to +3.3V via separate 3.3 KΩ resistor.

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PC•MIP Slot MAJ3

The following table shows the pin assignment of the PC•MIP Slot A rear I/O connector MAJ3 as well as the mapping to the *CompactPCI* rear I/O connector J5.

CompactPCI J5	MAJ3	Signal Name	Signal Name	MAJ3	*CompactPCI* J5
E13	1	I/O 01	I/O 02	2	D13
C13	3	I/O 03	I/O 04	4	B13
	5	GND	I/O 05	6	A13
E14	7	I/O 06	I/O 07	8	D14
C14	9	I/O 08	GND	10	
B14	11	I/O 09	I/O 10	12	A14
	13	GND	I/O 11	14	E15
D15	15	I/O 12	I/O 13	16	C15
B15	17	I/O 14	GND	18	
A15	19	I/O 15	I/O 16	20	E16
	21	GND	I/O 17	22	D16
C16	23	I/O 18	I/O 19	24	B16
A16	25	I/O 20	GND	26	
E17	27	I/O 21	I/O 22	28	D17
	29	GND	I/O 23	30	C17
B17	31	I/O 24	I/O 25	32	A17
E18	33	I/O 26	GND	34	
D18	35	I/O 27	I/O 28	36	C18
	37	GND	I/O 29	38	B18
A18	39	I/O 30	I/O 31	40	E19
D19	41	I/O 32	GND	42	
C19	43	I/O 33	I/O 34	44	B19
	45	GND	I/O 35	46	A19
E20	47	I/O 36	I/O 37	48	D20
C20	49	I/O 38	GND	50	
B20	51	I/O 39	I/O 40	52	A20
	53	GND	I/O 41	54	E21
D21	55	I/O 42	I/O 43	56	C21
B21	57	I/O 44	GND	58	
A21	59	I/O 45	I/O 46	60	E22
D22	61	I/O 47	I/O 48	62	C22
B22	63	I/O 49	I/O 50	64	A22

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PMC Slot MDJ1

MDJ1	Signal Name	Signal Name	MDJ1
1	*TCK*	-12V	2
3	GND	INTB# [1]	4
5	INTC# [1]	INTD# [1]	6
7	*BUSMODE1#*	+5V	8
9	INTA# [1]	*Reserved*	10
11	GND	+3.3V	12
13	CLK	GND	14
15	GND	GNT#	16
17	REQ#	+5V	18
19	VI/O [3]	AD31	20
21	AD28	AD27	22
23	AD25	GND	24
25	GND	C/BE3#	26
27	AD22	AD21	28
29	AD19	+5V	30
31	VI/O [3]	AD17	32
33	FRAME#	GND	34
35	GND	IRDY#	36
37	DEVSEL#	+5V	38
39	GND	LOCK#	40
41	*Reserved*	*Reserved*	42
43	PAR	GND	44
45	VI/O [3]	AD15	46
47	AD12	AD11	48
49	AD09	+5V	50
51	GND	C/BE0#	52
53	AD06	AD05	54
55	AD04	GND	56
57	VI/O [3]	AD03	58
59	AD02	AD01	60
61	AD00	+5V	62
63	GND	REQ64# [2]	64

pin positions printed italic/coloured brown: reserved by specification and not connected
pin positions printed italic/coloured blue: not connected on CD1-OPERA

Notes:

[1] This pin position is showing the actual interrupt assignment.

[2] This pin position is pulled to +3.3V via separate 3.3 KΩ resistor.

[3] $V_{I/O}$ is fixed to +3.3V on CD1-OPERA.

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PMC Slot MDJ2

MDJ2	Signal Name	Signal Name	MDJ2
1	+12V	*TRST#*	2
3	*TMS*	*TDO*	4
5	*TDI*	GND	6
7	GND	*Reserved*	8
9	SERIRQ [2)]	*Reserved*	10
11	BUSMODE2# [4)]	+3.3V	12
13	RST#	BUSMODE3# [4)]	14
15	+3.3V	BUSMODE4# [4)]	16
17	*PME#*	GND	18
19	AD30	AD29	20
21	GND	AD26	22
23	AD24	+3.3V	24
25	IDSEL [1)]	AD23	26
27	+3.3V	AD20	28
29	AD18	GND	30
31	AD16	C/BE2#	32
33	GND	*Reserved*	34
35	TRDY#	+3.3V	36
37	GND	STOP#	38
39	PERR#	GND	40
41	+3.3V	SERR#	42
43	C/BE1#	GND	44
45	AD14	AD13	46
47	*M66EN*	AD10	48
49	AD08	+3.3V	50
51	AD07	*Reserved*	52
53	+3.3V	*Reserved*	54
55	*Reserved*	GND	56
57	*Reserved*	*Reserved*	58
59	GND	*Reserved*	60
61	ACK64# [3)]	+3.3V	62
63	GND	*Reserved*	64

pin positions printed italic/coloured brown: reserved by specification and not connected
pin positions printed italic/coloured blue: not connected on CD1-OPERA

Notes:

1) IDSEL is assigned to AD28.

2) This pin position is normally a PMC reserved pin, on CD1 it may be used to connect to the SERIRQ signal.

3) This pin position is pulled to +3.3V via separate 3.3 KΩ resistor.

4) BUSMODE[4:2] signals coded according to P1386/Draft 2.4a pg. 48 (PCI Card) from CD1-OPERA Rev.2.1 off

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PMC Slot MDJ4

The following table shows the pin assignment of the PMC Slot rear I/O connector MDJ4 as well as the mapping to the *CompactPCI* rear I/O connector J5.

CompactPCI J5	MDJ4	Signal Name	Signal Name	MDJ4	*CompactPCI* J5
B15	1	I/O 01	I/O 02	2	C15
D15	3	I/O 03	I/O 04	4	E15
A14	5	I/O 05	I/O 06	6	B14
C14	7	I/O 07	I/O 08	8	D14
E14	9	I/O 09	I/O 10	10	A13
B13	11	I/O 11	I/O 12	12	C13
D13	13	I/O 13	I/O 14	14	E13
A11	15	I/O 15	I/O 16	16	B11
C11	17	I/O 17	I/O 18	18	D11
E11	19	I/O 19	I/O 20	20	A10
B10	21	I/O 21	I/O 22	22	C10
D10	23	I/O 23	I/O 24	24	E10
A9	25	I/O 25	I/O 26	26	B9
C9	27	I/O 27	I/O 28	28	D9
E9	29	I/O 29	I/O 30	30	A8
B8	31	I/O 31	I/O 32	32	C8
D8	33	I/O 33	I/O 34	34	E8
A7	35	I/O 35	I/O 36	36	B7
C7	37	I/O 37	I/O 38	38	D7
E7	39	I/O 39	I/O 40	40	A6
B6	41	I/O 41	I/O 42	42	C6
D6	43	I/O 43	I/O 44	44	E6
A5	45	I/O 45	I/O 46	46	B5
C5	47	I/O 47	I/O 48	48	D5
E5	49	I/O 49	I/O 50	50	A4
B4	51	I/O 51	I/O 52	52	C4
D4	53	I/O 53	I/O 54	54	E4
A3	55	I/O 55	I/O 56	56	B3
C3	57	I/O 57	I/O 58	58	D3
E3	59	I/O 59	I/O 60	60	A2
B2	61	I/O 61	I/O 62	62	C2
D2	63	I/O 63	I/O 64	64	E2

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The version of the CD1-OPERA prepared for use with an on-board hard disk drive maps the primary IDE port to MDJ4 as follows:

MDJ4	Signal Name	Signal Name	MDJ4
1	*NC*	*NC*	2
3	*NC*	*NC*	4
5	*NC*	*NC*	6
7	*NC*	*NC*	8
9	*NC*	*NC*	10
11	*NC*	*NC*	12
13	*NC*	*NC*	14
15	*NC*	*NC*	16
17	IDE D07	IDE RST#	18
19	*NC*	*NC*	20
21	*NC*	IDE D09	22
23	IDE D06	IDE D08	24
25	*NC*	*NC*	26
27	IDE D04	IDE D10	28
29	IDE D05	*NC*	30
31	*NC*	IDE D12	32
33	IDE D03	IDE D11	34
35	*NC*	*NC*	36
37	IDE D01	IDE D13	38
39	IDE D02	*NC*	40
41	*NC*	IDE D15	42
43	IDE D00	IDE D14	44
45	*NC*	*NC*	46
47	IDE CS0#	IDE CS1#	48
49	IDE ACT#	*NC*	50
51	*NC*	IDE A01	52
53	IDE A00	IDE A02	54
55	+5V	GND	56
57	IDE IORDY	IDE DACK#	58
59	INT (IRQ 14)	GND	60
61	+5V	IDE DREQ	62
63	IDE IOW#	IDE IOR#	64

pin positions printed italic/coloured brown: not connected

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CompactPCI J1

#J1	A	B	C	D	E
25	+5V	REQ64#	ENUM#	+3.3V	+5V
24	AD1	+5V	VI/O [3]	AD0	ACK64#
23	+3.3V	AD4	AD3	+5V [3]	AD2
22	AD7	GND	+3.3V [3]	AD6	AD5
21	+3.3V	AD9	AD8	*M66EN*	C/BE0#
20	AD12	GND	VI/O	AD11	AD10
19	+3.3V	AD15	AD14	GND	AD13
18	SERR#	GND	+3.3V	PAR	C/BE1#
17	+3.3V	IPMB SCL	IPMB SDA	GND	PERR#
16	DEVSEL#	GND	VI/O	STOP#	LOCK#
15	+3.3V	FRAME#	IRDY#	BDSEL# [4]	TRDY#
14	KEY AREA				
13					
12					
11	AD18	AD17	AD16	GND	C/BE2#
10	AD21	GND	+3.3V	AD20	AD19
9	C/BE3#	IDSEL [4]	AD23	GND	AD22
8	AD26	GND	VI/O	AD25	AD24
7	AD30	AD29	AD28	GND	AD27
6	REQ#	GND	+3.3V [3]	CLK	AD31
5	*BRSVP1A5*	*BRSVP1B5*	RST#	GND	GNT#
4	IPMB PWR	HEALTHY#	VI/O [3]	INTP [1]	INTS [2]
3	INTA#	INTB#	INTC#	+5V [3]	INTD#
2	*TCK*	+5V	*TMS*	*TDO*	*TDI*
1	+5V	-12V	*TRST#*	+12V	+5V

pin positions printed italic/coloured brown: Reserved by specification and not connected
pin positions printed italic/coloured blue: not connected

Notes:
[1] This pin is routed via a switch to IRQ14. See section "Interrupt Mapping" for details.
[2] This pin may be either IRQ15 or the SERIRQ line. See section "Interrupt Mapping" for details.
[3] This is a long pin providing an early connection on hot board insertion.
[4] This is a short pin providing the last connection on hot board insertion.

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CompactPCI J2

#J2	A	B	C	D	E
22	GA4 [1)]	GA3 [1)]	GA2 [1)]	GA1 [1)]	GA0 [1)]
21	CLK6	GND	*RSV*	*RSV*	*RSV*
20	CLK5	GND	*RSV*	GND	*RSV*
19	GND	GND	*RSV*	*RSV*	*RSV*
18	PXI TRIG3	PXI TRIG4	PXI TRIG5	GND	PXI TRIG6
17	PXI TRIG2	GND	PRST#	REQ6#	GNT6#
16	PXI TRIG1	PXI TRIG0	DEG#	GND	PXI TRIG7
15	*BRSVP2A15*	GND	FAL#	REQ5#	GNT5#
14	AD35	AD34	AD33	GND	AD32
13	AD38	GND	V(I/O)	AD37	AD36
12	AD42	AD41	AD40	GND	AD39
11	AD45	GND	V(I/O)	AD44	AD43
10	AD49	AD48	AD47	GND	AD46
9	AD52	GND	V(I/O)	AD51	AD50
8	AD56	AD55	AD54	GND	AD53
7	AD59	GND	V(I/O)	AD58	AD57
6	AD63	AD62	AD61	GND	AD60
5	C/BE5#	64EN#	V(I/O)	C/BE4#	PAR64
4	V(I/O)	*BRSVP2B4*	C/BE7#	GND	C/BE6#
3	CLK4	GND	GNT3#	REQ4#	GNT4#
2	CLK2	CLK3	SYSEN#	GNT2#	REQ3#
1	CLK1	GND	REQ1#	GNT1#	REQ2#

pin positions printed italic/coloured brown: not connected

[1)] The five geographic addressing lines GA0-4 are routed to the ICH4 GPIO32-36 respectively.

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CompactPCI J3

#J3	A	B	C	D	E
19	GND	GND	GND	GND	GND
18	LPa_DA+	LPa_DA-	GND	LPa_DC+	LPa_DC-
17	LPa_DB+	LPa_DB-	GND	LPa_DD+	LPa_DD-
16	*LPb_DA+*	*LPb_DA-*	GND	*LPb_DC+*	*LPb_DC-*
15	*LPb_DB+*	*LPb_DB-*	GND	*LPb_DD+*	*LPb_DD-*
14	GND	GND	GND	GND	GND
13	*NC*	*NC*	*NC*	*NC*	*NC*
12	*NC*	*NC*	*NC*	*NC*	*NC*
11	*NC*	*NC*	*NC*	*NC*	*NC*
10	*NC*	*NC*	*NC*	*NC*	*NC*
9	*NC*	*NC*	*NC*	*NC*	*NC*
8	*NC*	*NC*	*NC*	*NC*	*NC*
7	*NC*	*NC*	*NC*	*NC*	*NC*
6	*NC*	*NC*	*NC*	*NC*	*NC*
5	*NC*	*NC*	*NC*	*NC*	*NC*
4	*NC*	*NC*	*NC*	*NC*	*NC*
3	*NC*	*NC*	*NC*	*NC*	*NC*
2	*NC*	*NC*	*NC*	*NC*	*NC*
1	*NC*	*NC*	*NC*	*NC*	*NC*

pin positions printed italic/coloured brown: not connected
pin positions printed italic/coloured blue: not connected

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CompactPCI J4

#J4	A	B	C	D	E
25	*NC*	GPIO8	GPIO12	*NC*	USB P2+
24	*NC*	GPIO9	GPIO13	*NC*	USB P2-
23	*NC*	GPIO10	GPIO14	*NC*	USB P1+
22	COM2 RI#	GPIO11	GPIO15	+5V	USB P1-
21	COM2 RTS#	COM2 DSR#	COM2 CTS#	COM2 DCD#	USB OC#
20	*NC*	+5V	COM2 TXD	COM2 RXD	COM2 DTR#
19	GND	GND	*NC*	*NC*	*NC*
18	LPT PE	LPT SLCT	+5V	GND	*NC*
17	LPT D05	LPT D06	LPT D07	LPT ACK#	LPT BUSY
16	LPT INIT#	LPT D02	LPT SLCTIN#	LPT D03	LPT D04
15	LPT STROBE#	LPT ALF#	LPT D00	LPT ERROR#	LPT D01
14					
13			KEY AREA		
12					
11	FD TRK0#	FD WRTPRT#	FD RDATA#	FD HDSEL#	FD DSKCHG#
10	GND	FD DIR#	FD STEP#	FD WDATA#	FD WGATE#
9	FD DRVDEN0#	FD INDEX#	FD MTR0#	GND	FD DS0#
8	+5V	GND	+12V	GND	+12V
7	+5V	IDE CS1#	GND	IDE CS3#	IDE ACT#
6	IDE DACK#	IDE IRQ14	IDE A01	IDE A00	IDE A02
5	GND	IDE IOW#	GND	IDE IOR#	IDE IORDY
4	IDE D14	IDE D00	IDE D15	GND	IDE DREQ
3	IDE D03	IDE D12	IDE D02	IDE D13	IDE D01
2	IDE D09	IDE D05	IDE D10	IDE D04	IDE D11
1	IDE RST#	GND	IDE D07	IDE D08	IDE D06

pin positions printed italic/coloured brown: not connected

[1] The IDE signals belong to the primary IDE interface of the CD1-OPERA.
[2] The COM2 interface is routed also to the header JSAM. Only one of both interfaces should be used at the same time.
[3] The GPIOs are controlled by the PCI-PXI bridge similar to the GPIOs on the header JSAM.
[4] The signals on row 1 to 7 of J4 are not available on the CD1-OPERA version prepared for on-board hard disk drive.

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CompactPCI J5

The next table shows the mapping of the rear I/O signals of the PC•MIP Slot A respective the PMC module to the *CompactPCI* connector J5. The value in a column gives the PC•MIP module's J3 pin number or the PMC module's J4 pin number where the I/O signal originates. Example: On J5 pin B15 occurs the I/O signal coming from PC•MIP module MAJ3 pin 17 or from PMC module MDJ4 pin 1 respectively.

#J5	A	B	C	D	E
22	MAJ3.64	MAJ3.63	MAJ3.62	MAJ3.61	MAJ3.60
21	MAJ3.59	MAJ3.57	MAJ3.56	MAJ3.55	MAJ3.54
20	MAJ3.52	MAJ3.51	MAJ3.49	MAJ3.48	MAJ3.47
19	MAJ3.46	MAJ3.44	MAJ3.43	MAJ3.41	MAJ3.40
18	MAJ3.39	MAJ3.38	MAJ3.36	MAJ3.35	MAJ3.33
17	MAJ3.32	MAJ3.31	MAJ3.30	MAJ3.28	MAJ3.27
16	MAJ3.25	MAJ3.24	MAJ3.23	MAJ3.22	MAJ3.20
15	MAJ3.19	MAJ3.17/MDJ4.1	MAJ3.16/MDJ4.2	MAJ3.15/MDJ4.3	MAJ3.14/MDJ4.4
14	MAJ3.12/MDJ4.5	MAJ3.11/MDJ4.6	MAJ3.9/MDJ4.7	MAJ3.8/MDJ4.8	MAJ3.7/MDJ4.9
13	MAJ3.6/MDJ4.10	MAJ3.4/MDJ4.11	MAJ3.3/MDJ4.12	MAJ3.2/MDJ4.13	MAJ3.1/MDJ4.14
12	+3.3V	+3.3V	+3.3V	+5V	+5V
11	MDJ4.15	MDJ4.16	MDJ4.17	MDJ4.18	MDJ4.19
10	MDJ4.20	MDJ4.21	MDJ4.22	MDJ4.23	MDJ4.24
9	MDJ4.25	MDJ4.26	MDJ4.27	MDJ4.28	MDJ4.29
8	MDJ4.30	MDJ4.31	MDJ4.32	MDJ4.33	MDJ4.34
7	MDJ4.35	MDJ4.36	MDJ4.37	MDJ4.38	MDJ4.39
6	MDJ4.40	MDJ4.41	MDJ4.42	MDJ4.43	MDJ4.44
5	MDJ4.45	MDJ4.46	MDJ4.47	MDJ4.48	MDJ4.49
4	MDJ4.50	MDJ4.51	MDJ4.52	MDJ4.53	MDJ4.54
3	MDJ4.55	MDJ4.56	MDJ4.57	MDJ4.58	MDJ4.59
2	MDJ4.60	MDJ4.61	MDJ4.62	MDJ4.63	MDJ4.64
1	+3.3V	+3.3V	+3.3V	+5V	+5V

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Power Supply Requirements

Operating Voltage	min./max. current P4-M 1.7GHz	min./max. current P4-M 2.2GHz	min./max. current P4-M 1.2GHz [1)]
+5V (+0.25V/-0.15V)	0.9A/5.4A	1.1A/7.2A	0.7A/3.2A
+3.3V (+0.17V/-0.10V)	2.2A/2.9A	2.2A/2.9A	2.2A/2.9A
+12V (±0.6V)	0/0 [2)]	0/0 [2)]	0/0 [2)]
-12V (±0.6V)	0/0 [2)]	0/0 [2)]	0/0 [2)]

[1)] This is the speed of the so called Battery Optimized Mode that any P4-M processor enters after reset.
[2)] This voltage is not necessary to operate the CD1-OPERA.

Literature

Theme	Document Title	Origin
CompactPCI Specification	*CompactPCI* Specification, PICMG 2.0 R3.0, Oct. 1, 1999	PICMG (http://www.picmg.org)
CompactPCI Hot Swap	*CompactPCI* Hot Swap Specification, PICMG 2.1 R2.0, Jan. 17, 2001	PICMG (http://www.picmg.org)
CompactPCI Backplane Ethernet	*CompactPCI* Packet Switching Backplane Specification, PICMG 2.16 R1.0, Sept. 5, 2001	PICMG (http://www.picmg.org)
PCI	PCI Hardware and Software Architecture & Design, Solari/Willse, 4th Edition, Annabooks	Annabooks (http://www.annabooks.com)
USB Specification	Universal Serial Bus Specification	http://www.teleport.com/~usb
Metric Connectors	IEC 1076-4-101 Application Literature from ERNI, AMP, FCI	Beuth Verlag, Berlin ILI Index House, GB SL57EU Ascot Berkshire
2.54mm Shrouded Headers	DIN 41651	Beuth Verlag, Berlin
CompactFlash Specification	CompactFlash Specification R1.4	http://www.compactflash.org

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